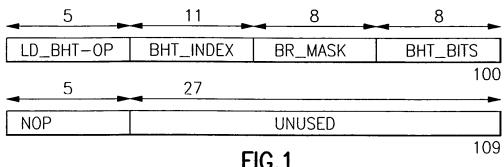
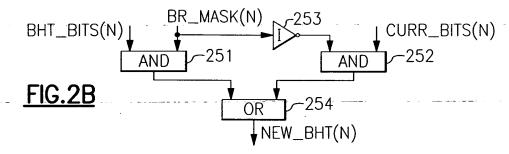
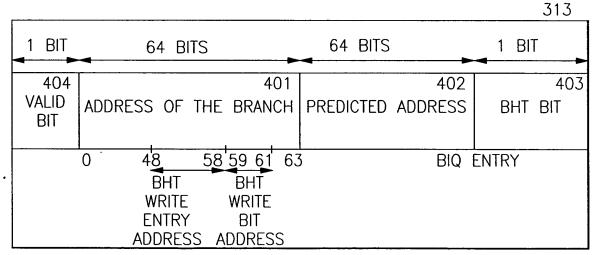


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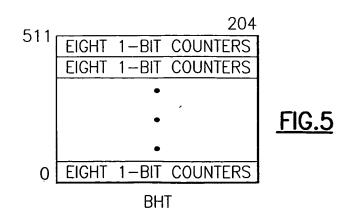
## FIG.1





BRANCH INFORMATION QUEUE (BIQ)

## FIG.4





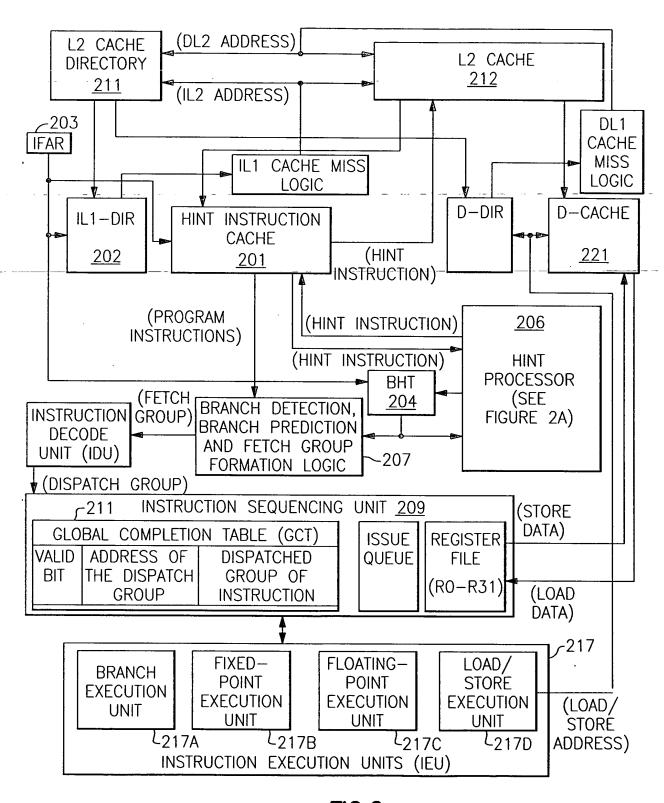
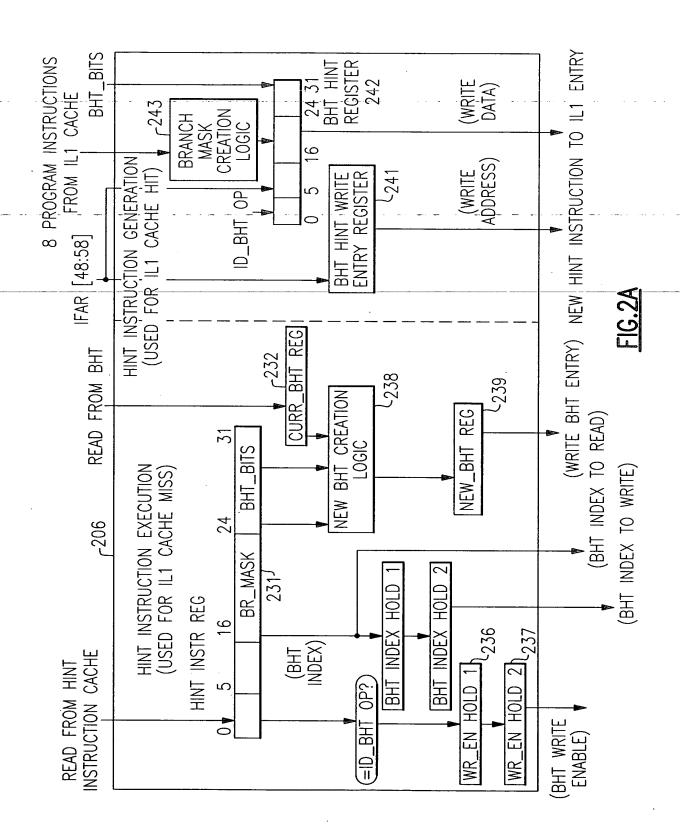
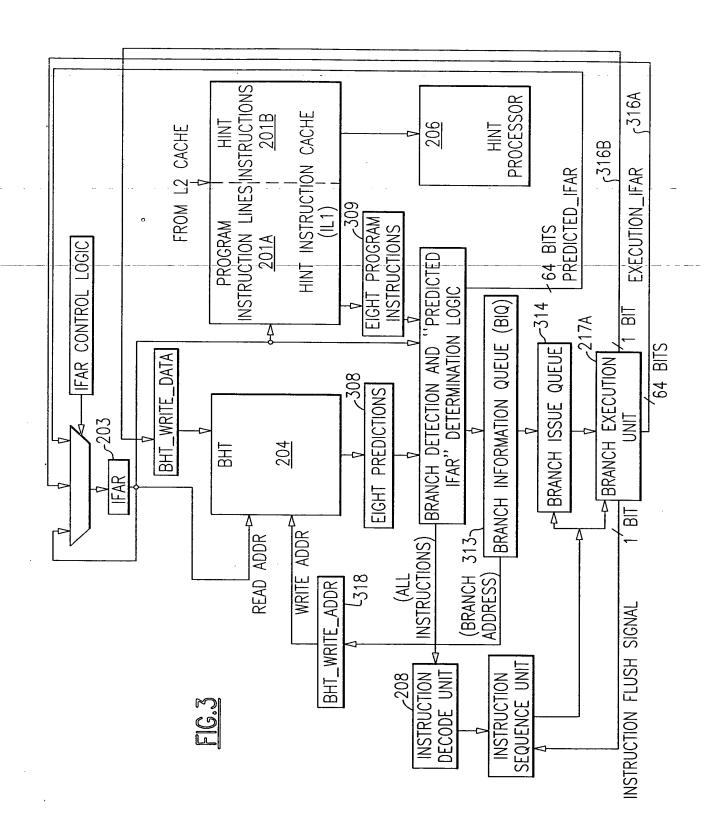


FIG.2

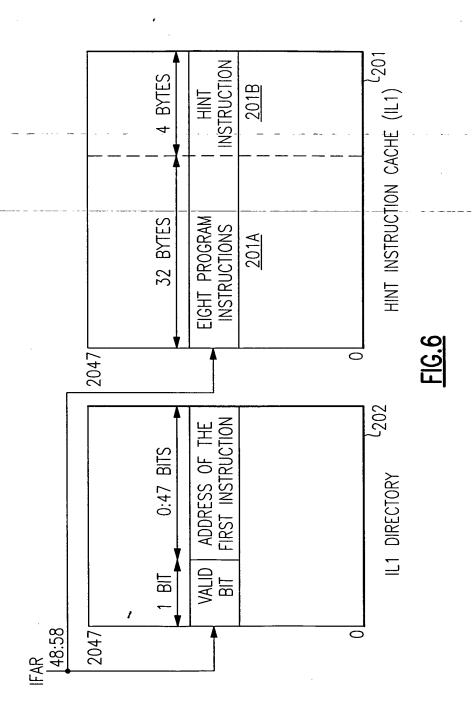




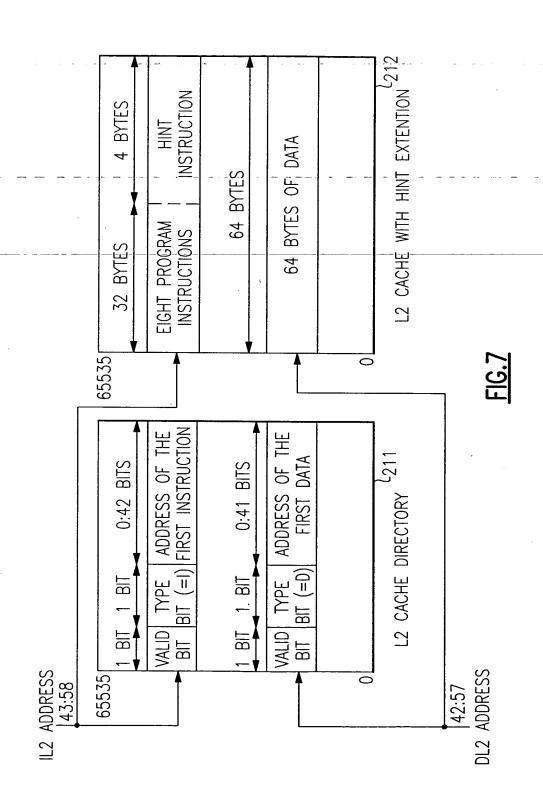




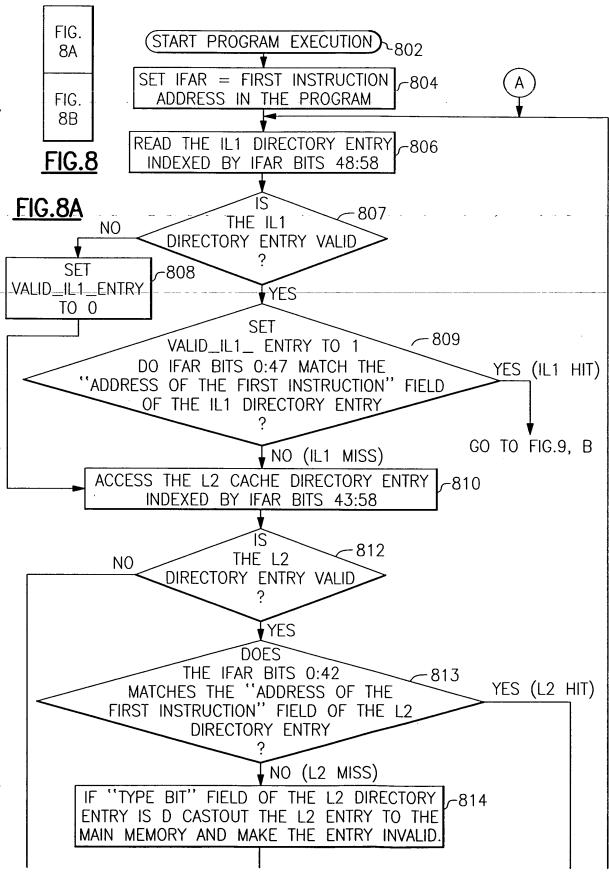














READ THE INSTRUCTIONS FROM THE MAIN MEMORY AND LOAD | 815 THE L2 CACHE AND VALIDATE THE L2 DIRECTORY ENTRY. MAKE THE HINT INSTRUCTION IN THE L2 CACHE ENTRY NOP. IS 817 NO. VALID\_IL1\_ENTRY = 1<del>--</del>816 ∛YES ASSIGN "-IL1\_-HINT\_-WR\_-ADDR" AS -THE IL1- INDEX EQUAL- TO IFAR BITS 48:58 ASSIGN "IL2\_HINT\_WR ADDR" AS THE L2 INDEX EQUAL TO THE CONCENTRATION OF BITS 43:47 OF THE "ADDRESS OF THE -FIRST-INSTRUCTION''- FIELD-OF-THE-1-CACHE-DIRECTORY-ENTRY INDEXED BY IL1\_HINT\_WR\_ADDR WITH IFAR BITS 48:58. ACCESS THE L2 DIRECTORY ENTRY INDEXED BY IL2\_HINT\_WR\_ADDR IS THE L2 ENTRY VALID, -818 AND DOES ITS "ADDRESS OF THE FIRST INSTRUCTION" FIELD MATCH BITS 0:47 OF NO. THE "ADDRESS OF THE FIRST INSTRUCTION" FIELD OF THE IL1 DIRECTORY ENTRY INDEXED BY IL1\_HINT\_WR\_ADDR AND ITS "TYPE BIT" FIELD=I YES (ENTRY BEING REPLACED 820 ~ IN IL1 HAS COPY IN L2) WRITE THE 4-BYTE HINT INSTRUCTION FROM THE I-CACHE ENTRY INDEXED BY IFAR BITS 48:58 INTO HINT INSTRUCTION FIELD OF THE L2 CACHE ENTRY INDEXED BY THE IL2\_HINT\_WR\_ADDR 822 -LOAD THE IL1 ENTRY WITH 8 PROGRAM INSTRUCTIONS FROM "EIGHT PROGRAM INSTRUCTIONS" FIELD AND THE HINT INSTR OF THE ENTRY IN L2 CACHE INDEXED BY IFAR BITS 43:58 FORWARD THE HINT INSTRUCTION TO THE HINT PROCESSOR AND EXECUTE THEM (SEE FIGURE 13)

<u>FIG.8B</u>



901<sub>5</sub> B FROM FIGURE 8.

FETCH THE IL1 CACHE LINE INTO "EIGHT PROGRAM INSTRUCTIONS" REGISTER, AND THE ASSOCIATED HINT INSTRUCTIONS IN THE HINT INSTRUCTION REGISTER.

ACCESS THE BHT ENTRY INDEXED BY THE IFAR BITS 48:58, AND FETCH ITS BHT PREDICTION BITS INTO THE "EIGHT PREDICTIONS" REGISTER.

USE THE IFAR BITS 59:61 TO LOCATE "FIRST INSTRUCTION" IN THE "EIGHT PROGRAM INSTRUCTIONS" REGISTER. (INSTRUCTIONS BEFORE THE "FIRST INSTRUCTION", IF ANY, WILL BE IGNORED).

THERE ANY BRANCH

YES INSTRUCTION IN THE "EIGHT PROGRAM INSTRUCTIONS" REGISTER AT OR AFTER THE "FIRST INSTRUCTION"

?

906 NO

DESIGNATE A "FETCH GROUP" AS THE INSTRUCTIONS FROM THE

DESIGNATE A "FETCH GROUP" AS THE INSTRUCTIONS FROM THE "FIRST INSTRUCTION" TO THE END OF THE REGISTER. SET "PREDICTED\_IFAR" TO THE ADDRESS OF THE NEXT SEQUENTIAL INSTRUCTION AFTER THE "FETCH GROUP".

IN THE HINT PROCESSOR, FILL THE BHT HINT REGISTER WITH THE FOLLOWING: BITS 0:4 WITH "ID\_BHT\_OP", BITS 5:15 WITH IFAR BITS 48:58, BITS 16:23 WITH A 8-BIT "BRANCH MASK" FIELD CONTAIN-ING A 1 IN THE POSITIONS WHERE THERE IS A BRANCH AND 0 IN OTHER POSITIONS, BITS 24:31 WITH THE 8-BIT BHT PREDICTION.

IN THE HINT PROCESSOR, STORE IFAR BITS 48:58 IN THE BHT HINT WRITE ENTRY REGISTER

STORE THE CONTENT OF THE BHT HINT REGISTER IN THE HINT INSTRUCTION FIELD IN THE IL1 CACHE AT THE LOCATION IN THE BHT HINT WRITE ENTRY REGISTER

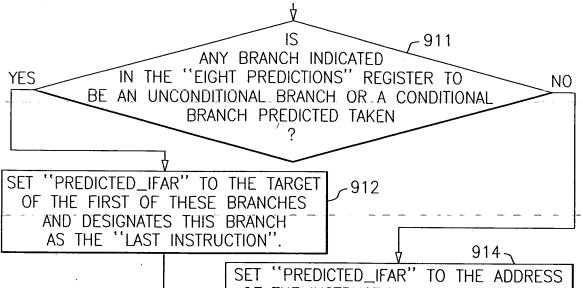
FIG. 9A

FIG. 9B

FIG. 9B

FIG. 9B





SET "PREDICTED\_IFAR" TO THE ADDRESS
OF THE INSTRUCTION NEXT SEQUENTIAL
TO THE LAST INSTRUCTION FETCHED.
DESIGNATE THE LAST INSTRUCTION IN THE
"EIGHT INSTRUCTIONS" REGISTER AS
THE "LAST INSTRUCTION".

 $921_{1}$ 

ALL INSTRUCTIONS BETWEEN THE "FIRST INSTRUCTION" AND THE "LAST INSTRUCTION" FORMS THE "FETCH GROUP".

FOR EACH BRANCH IN FETCH GROUP, OBTAIN AN INVALID ENTRY IN THE BRANCH INFORMATION QUEUE (BIQ), SET ITS VALID BIT TO 1 STATE AND PUT:

THE ADDRESS OF THE BRANCH IN THE "ADDRESS OF THE BRANCH" FIELD,

THE BRANCH TARGET ADDRESS IN THE "PREDICTED ADDRESS" FIELD IF THE BRANCH IS PREDICTED TAKEN OR THE SEQUENTIAL ADDRESS IN THE "PREDICTED ADDRESS" FIELD IF THE BRANCH IS PREDICTED NOT—TAKEN,

IF THE BRANCH IS AT POSITION "N", STORE
THE N-TH BIT IN THE "EIGHT PREDICTIONS" REGISTER IN
THE "BHT BIT" FIELD.

PLACE THE BRANCH IN THE BRANCH ISSUE QUEUE FOR ITS SUBSEQUENT EXECUTION.

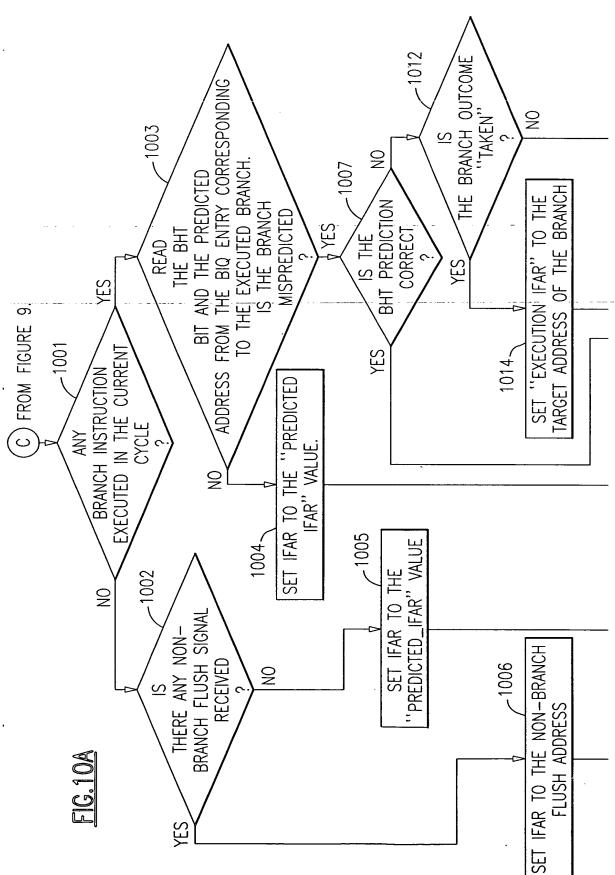
926

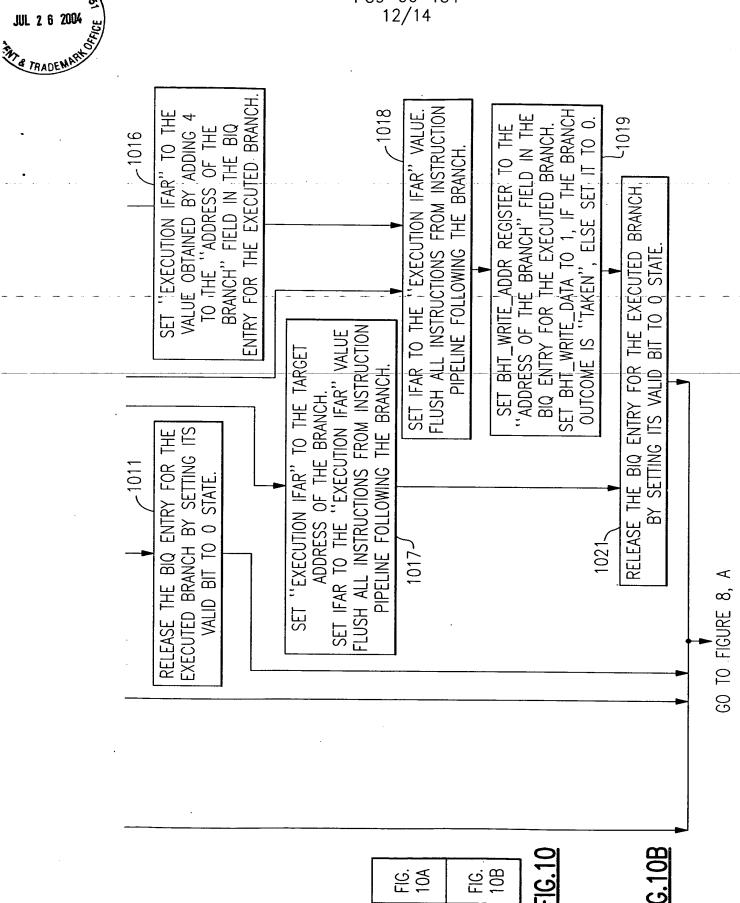
FORWARD THE FETCH GROUP TO INSTRUCTION DECODE UNIT (IDU), SEE FIGURE 11.

FIG.9B

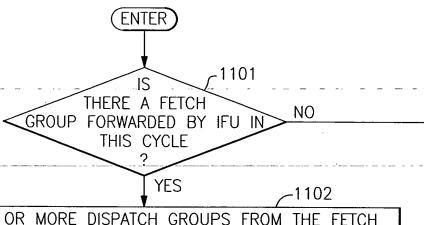
GO TO FIGURE 10, C











FORM ONE OR MORE DISPATCH GROUPS FROM THE FETCH GROUP RECEIVED BY THE IDU FROM IFU FOLLOWING THE RULES OF DISPATCH GROUP FORMATION (NOT MORE THAN FIVE INSTRUCTIONS PER GROUP, AT MOST ONE BRANCH IN THE DISPATCH GROUP, FIFTH SLOT IN THE DISPATCH GROUP IS RESERVED FOR BRANCH INSTRUCTIONS ONLY AND IF THERE IS NOT ENOUGH INSTRUCTIONS TO FILL ALL THE SLOTS IN THE DISPATCH GROUP, INSERT NOPs)

OBTAIN AN INVALID ENTRY IN THE GLOBAL COMPLETION TABLE (GCT) AND FILL ITS FIELD WITH THE INFORMATION FOR THE DISPATCH GROUP AND VALIDATE THE ENTRY PLACE EACH OF THE INSTRUCTIONS IN THE DISPATCH GROUP IN THE ISSUE QUEUE FOR SUBSEQUENT EXECUTION (SEE FIGURE 12)

**EXIT** 

**FIG.11** 



